

# Jeremy W. Webb

---

921 Tufts Place, Woodland, CA 95695  
Cellular: (530) 604-2456

E-mail: jeremy.webb@ieee.org  
Website: jwebb-design.com

## **OBJECTIVE**

To obtain a full-time position as a Senior Electrical Engineer in the field of Digital Signal Processing and Communications.

## **ENGINEERING EXPERTISE**

### **Design**

- FPGA and CPLD Logic design in Verilog and SystemVerilog: Altera and Xilinx devices.
- High-speed digital PC board design: up to 16 GHz, single-ended and differential transmission lines, LVPECL, ECL, LVDS, CML.
- Microprocessors: IBM PowerPC 405GPr, Microchip, Xilinx PicoBlaze and MicroBlaze.
- Highly skilled at circuit and system initial turn-on and debug.

### **Measurement**

- Logic Analyzer, Digital Communications Analyzer, Oscilloscope, Bit Error Rate Tester (BERT), Pulse Generator, Spectrum Analyzer, Signal Source, Network Analyzer, Serial Component Monitor.

### **CAE**

- Mentor Graphics Board Station/PADS/DxDesigner, PSPICE/HSPICE/HPSPICE, Agilent ADS, AutoCAD R14/2000/2002, Synplicity Synplify Pro/Premier, ModelSim, Questa, Xilinx ISE/EDK/PlanAhead/ChipScope, Altera Quartus II, MATLAB, Aldec Active-HDL/Riviera-PRO, Synopsys DC Compiler, Genesys Filter SW, Orcad Schematic Capture, and Orcad Layout Plus.

### **Programming**

- SystemVerilog, Verilog HDL, MATLAB, C, Assembly, VEE, Visual Basic, VHDL, Perl, Tcl/Tk, L<sup>A</sup>T<sub>E</sub>X.

---

## **PROFESSIONAL EXPERIENCE**

**Centellax, Santa Rosa, CA**

**April 2007–Present**

**Senior Design Engineer**

- Designed the Data Path FPGAs for the PG32 32Gb/s Programmable Pattern Generator and ED32 32Gb/s Programmable Error Detector PODs. The Data Path FPGAs operate at speeds up to 1Gb/s, interface with 4 16:1 Multiplexers and 1:16 Demultiplexers operating at 8Gb/s, and generate both Pseudo-Random Binary Sequences and custom user patterns.
- Architected the Data Path FPGAs for the PPG12500 10Gb/s Programmable Pattern Generator and PED12500 10Gb/s Programmable Error Detector. The Data Path FPGA operates at speeds up to 1Gb/s, interfaces with 36Mb of QDR-II SRAM operating at 500Mb/s, and generates both Pseudo-Random Binary Sequences and custom user patterns.
- Designed the Xilinx MicroBlaze Hardware Architecture used on digital sub-systems. The MicroBlaze 32-bit processors had many peripherals including a 512Mb 125MHz DDR2 SDRAM, 2GB microSD card, and 64Mb SPI Flash PROM.
- Documented FPGA and PC board designs using a combination of an internal wiki and website and an engineering reference specification. The documents contained information on design intent, control algorithms, register definitions, and hardware modifications.
- Performed software design of control algorithms using C code for loading patterns and capturing data. The C code interfaced to a Xilinx Virtex-5 FPGA via a 32-bit MicroBlaze processor running in a Xilinx Spartan-3A DSP FPGA.

- Managed the development effort for an external PC application used to load custom patterns onto Centellax PPG12500, PED12500, and PCB12500 products. Specified requirements for software functionality and user interface design.
- Created a web based search utility to simplify company-wide part searches using a combination of Perl DBM and CGI.
- Streamlined new part number requests by implementing a web-based submission form which automatically distributed the part information to the appropriate departments and personnel. As a result, part setup mistakes on printed circuit boards and mechanical drawings were minimized.

**University of California, Davis, Davis, CA**  
**Research Assistant**

**October 2003–March 2011**

- Architected a baseband signal source and spectrum analyzer instrument capable of generating or analyzing signals in the frequency range of DC to 125 MHz. The signal source is capable of generating either CW signals or arbitrary waveforms.
- Designed a configuration interface for a first- and second-generation multi-core processor.
- Developed a website to document the progress and design process of my Masters thesis project. Created a Subversion revision control repository for tracking all design files from PC board schematics to SystemVerilog code for FPGA designs.
- Mentored several undergraduate students in various disciplines including embedded software design, FPGA design, and PC board design.
- Consulted for several UC Davis research groups including the Chemistry Department, the Mechanical Engineering Department, and the Optical Research Group. Provided information regarding FPGA and embedded software design.

**Agilent Technologies, Inc., Santa Rosa, CA**  
**Hardware Design Engineer**

**October 2004–April 2007**

- Implemented a high-performance numerically controlled oscillator for a Direct Digital Clock Synthesizer in a Xilinx Virtex II and Virtex-4 FPGA.
- Performed schematic design for a high-performance Spectrum Analyzer Motherboard.
- Proposed and built an RS-232 Hub/SPI Controller board for a high-performance Spectrum Analyzer. This board allowed for faster debug and turn-on of SA Measurement boards.
- Responsible for multiple complex designs targeting multi-million gate FPGAs.
- Led the schematic design and layout of the analog section of a new measurement board for a high-performance Spectrum Analyzer, thus accelerating the schedule by 2 months.

**Thomson Grass Valley, Nevada City, CA**  
**Hardware Design Engineer**

**July 2004–October 2004**

- Implemented an SDRAM controller for a Filter Control FPGA in a Video Production Box.

**Barco-Folsom, LLC., Rancho Cordova, CA**  
**Hardware Design Engineer**

**January 2004–July 2004**

- Designed the motherboard for the new Folsom Research controller. The project involved PC board and FPGA Verilog HDL core design using a Xilinx Spartan IIE. The FPGA interfaced to an IBM PowerPC, a MultiMedia Card, USB, RS-232, a PS/2 keyboard, Ethernet, and an ADC.

**Folsom Research, Inc., Rancho Cordova, CA**  
**Hardware Design Engineer**

**March 2003–January 2004**

- Developed FPGA Verilog HDL cores and PC Boards for Audio and Video presentation systems.

**Agilent Technologies, Inc., Santa Rosa, CA**  
**Manufacturing Development Engineer**

**July 2001–October 2002**

- Created test specifications for PC boards, assisted with environmental qualification and testing, trained technicians on troubleshooting to reduce scrap costs for Agilent's 86130A BitAnalyzer, N1015A Modulation Test Set, and 71501D Jitter Analysis System.

**Agilent Technologies, Inc., Santa Rosa, CA**  
**Hardware Design Engineer**

**October 2000–July 2001**

- Designed and manufactured a demonstration tool (JET) for Agilent's 86130A BitAnalyzer. The project involved PC board and FPGA Verilog HDL core design using Xilinx Spartan II FPGAs. The JET helped to increase customer understanding of the BitAnalyzers Error Analysis Software and resulted in increased sales.
- Presented a poster paper on the effectiveness of Agilent's 86130A Error Analysis software at the Optical Network Interface Design Symposium 2002 in San Jose, CA.  
<http://jwebb-design.com/publications.html>

**Agilent Technologies, Inc., Santa Rosa, CA**  
**Intern**

**July 2000–September 2000**

- Co-designed and assembled a 10 GHz phase-locked YIG signal source. Involved designing C and Assembly language software modules to interface a PIC microprocessor, DACs, and a fractional-n synthesizer.

---

## **EDUCATION**

- **M.S.E.E., University of California, Davis**—March 2011
  - Emphasis on digital signal processing design.
  - Thesis project: A High Performance Baseband Instrument
- **B.S.E.E., University of California, Davis**—June 2000
  - Emphasis on signal processing and communications design.

## **AWARDS AND PUBLICATIONS**

- Recipient of an Agilent Technologies 2006 Innovation Merit Award for my idea entitled: "FPGA Design Creation Automation".
  - I designed many Perl scripts and Makefiles to automate various parts of the programmable logic design cycle.
- Agilent 86130A Error Analysis Demonstration poster paper, ONIDS 2002
  - Received Agilent Technologies Author Recognition award.
- 10 GHz Phase-Locked YIG Source, UC Davis Prized Writing contest, 2001-2002
  - Received Honorable Mention recognition.
- Jeremy W. Webb, "A High Performance Baseband Instrument", Masters Thesis, Technical Report ECE-VCL-2011-3, VLSI Computation Laboratory, ECE Department, University of California, Davis, 2011.

- Dean N. Truong, Wayne H. Cheng, Tinoosh Mohsenin, Zhiyi Yu, Anthony T. Jacobson, Gouri Landge, Michael J. Meeuwsen, Anh T. Tran, Zhibin Xiao, Eric W. Work, Jeremy W. Webb, Paul V. Mejia, Bevan M. Baas, "A 167-Processor Computational Platform in 65 nm CMOS" IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 4, pp. 1130-1144, April 2009.
- Dean Truong, Wayne Cheng, Tinoosh Mohsenin, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas. "A 167-processor Computational Array for Highly-Efficient DSP and Embedded Application Processing." In Proceedings of the IEEE HotChips Symposium on High-Performance Chips (HotChips 2008), August 2008.
- Dean Truong, Wayne Cheng, Tinoosh Mohsenin, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan M. Baas. "A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling." Symposium on VLSI Circuits, (VLSI '08), June 2008, pp. 22-23.
- Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Tinoosh Mohsenin, Bevan Baas, "Architecture and Evaluation of an Asynchronous Array of Simple Processors," Journal of VLSI Signal Processing Systems, March 2008.
- Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Dean Truong, Tinoosh Mohsenin, Bevan Baas, "AsAP: An Asynchronous Array of Simple Processors," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 3, pp. 695-705, March 2008.
- Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Tinoosh Mohsenin, Dean Truong, Jason Cheung "AsAP: A Fine-grain Multi-core Platform for DSP Applications," IEEE Micro, Volume 27, Number 2, March/April 2007.
- Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Daniel Gurman, Chi Chen, Jason Cheung, Tinoosh Mohsenin. "Hardware and Applications of AsAP: An Asynchronous Array of Simple Processors." In Proceedings of the IEEE HotChips Symposium on High-Performance Chips (HotChips 2006), August 2006.
- Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Tinoosh Mohsenin, Mandeep Singh, Bevan M. Baas. "An Asynchronous Array of Simple Processors for DSP Applications." In Proceedings of the IEEE International Solid-State Circuits Conference, (ISSCC '06) , February 2006, pp.428-429.